**CSC 3100 Final Exam**

A diagram of a state

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Figure Q1 -1 – State Diagram for Question 1

Output z = NOT( x)  
I mean look at the transition table, it’s always 1 when x is 0, and always 0 when x is 1.

A diagram of a circuit

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A and B represent the state (the little rectangles that store values have them as inputs), and there combinations represent the 4 stages of the state.

|  |  |  |
| --- | --- | --- |
| A | B | State |
| 0 | 0 | A |
| 0 | 1 | B |
| 1 | 0 | C |
| 1 | 1 | D |

A belongs to a JK flip flop, with B for K (reset) and X for J (input) . For a JK flip flopwhen both inputs are 0, the current state remains, when K = 1, the state returns to zero, when J is 1 and and K is 0, the state becomes 1, when both JK =1, then the current state flips.   
  
B is part of a T flip flop, where when the input changes to 1 FROM ZERO, the current state toggles to the opposite. That really makes drawing this state diagram more confusing – to draw it more simply I am going to interpret the toggle as indicating a flip. The input T is either X or NOT(A)  
  
If I am reading this right, Z = (A’X) OR (AX’B)

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A | A' | B | B’ | X = J | B = X’ | T = X OR A’ | A’ | B’ |
| 0 | 1 | 0 | **1** | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | **1** | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | **0** | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | **0** | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | **1** | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | **1** | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | **0** | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | **0** | 1 | 0 | 1 | 1 | 0 |

A diagram of a number of circles and numbers

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Figure Q2 – State diagram for question 2. Note that T previous has ALWAYS been assumed to be 0 for the sake of convenience when drawing.   
  
A diagram of a circuit

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X is the result of a DG latch, when G is up (=1), the latch is transparent, meaning outputs change on current inputs. When G is down(=0), the previous input is retained REGARDLESS of change in A.

Z is the result of a JK flip flop, For a JK flip flop when both inputs are 0, the current state remains, when K = 1, the state returns to zero, when J is 1 and and K is 0, the state becomes 1, when both JK =1, then the current state flips. X is J, and NOT X is K. The JK flip flop is attached to the falling clock edge.

A drawing of a diagram

Description automatically generated with medium confidence

Figure Q3 – Timing Diagram for Question 3  
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The moore machine has two input signals, X and NOT Clear, but only 1 output Q. This means it only has 1 state: Q = 0 and Q =1, however it has 4 inputs. The moore machine is FALLING edge triggered.

The mealy machine is the same as the previous, except with a XOR gate for Y and X.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| X | Clear | Clear’ | Y | Z = X XOR Y |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |

A drawing of a bird

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Figure Q4A – State Diagram for 4A

A drawing of a diagram

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Figure Q4B – The state diagram for 4B  
  
A diagram of a graph

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Figure Q4C – Waveform Diagram for Question 4

A diagram of a circuit

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Ok, let’s read this over. G is already given as a string of numbers and is unchanging, but the input for D is dependent ALWAYS on the output of Q3. Every single latch is rising edge triggered, and is a XOR for the data input, meaning ONLY ONE input must be one for 1 to pass. When the enable input is 1, the enable trigger passes D to Q, otherwise if it is 0 it holds its last previous input. I am very confused by reset remaining high, wouldn’t that mean that after the initial change in value the stored value is reset to 0? OH WAIT THERE’S THE LITTLE CIRCLE, WHY DO YOU KEEP PUTTING THOSE THERE I NEVER SEE THEM.

A diagram of a machine

Description automatically generated

Figure Q5-???- Inputting G values to simplify thinking. Let’s write out a XOR table to simplify thinking even further.

|  |  |  |
| --- | --- | --- |
| A | B | A XOR B |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

I am too confused to keep track of this, I’m going to create a bulk solution truth table.

A grid of numbers and letters

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There we go. No more thinking necessary, every single thought has been taken care of. REMEMBER, THE VALUES PASS IMMEDIATELY BASED ON PREVIOUS VALUES BECAUSE THEY ARE BASED ON CLOCK EDGE.  
A diagram with numbers and lines

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Figure 5?? – Calculated values for Q in each period.

A diagram of a circuit

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A diagram of a circuit

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Figure Q5-1 Diagramming circuit MUX so I don’t have to think hard when writing the equations. Ignore the fact that I mixed up the shape of AND OR for the first two. OR is the pointy one.

A.) F = (X OR Y)Z OR XYZ’

B.) F = (Y OR Z)X OR X’YZ

C.)F = (X OR Z)Y OR XY’Z